



# GK7205V210 Datasheet

**Version 1.1**

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## Version History

Version	Note
V0.1	Initial Version
V0.2	Format Adjustment
V0.3	Add Order Notes
V1.1	Additional hardware features

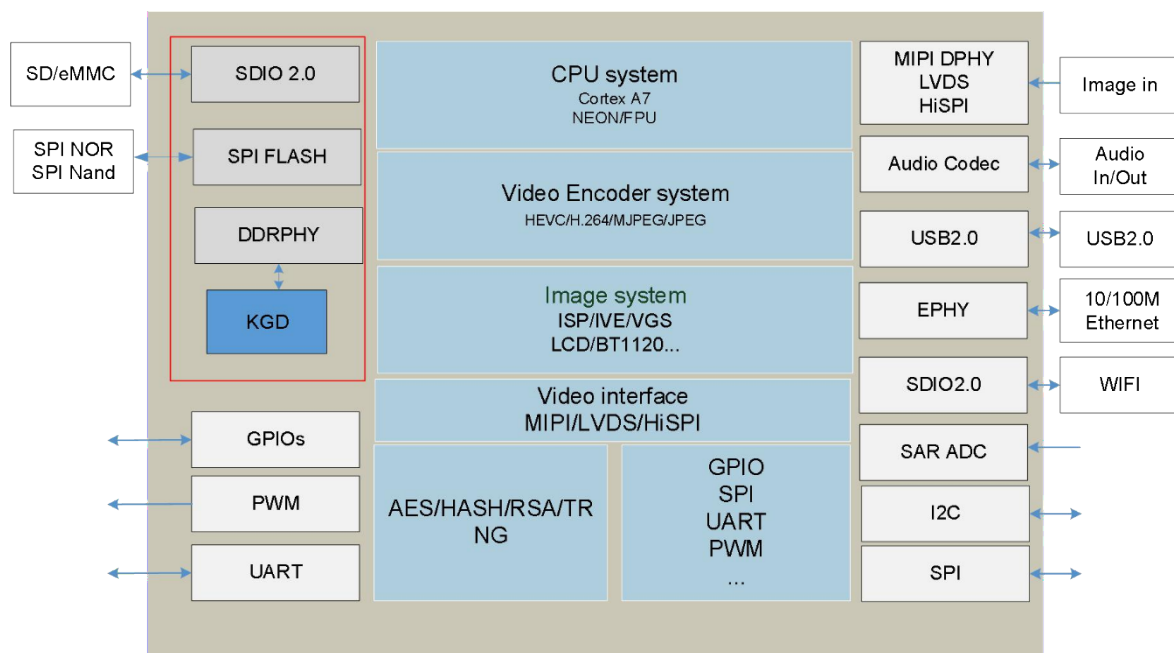
## Catalog

<b>Version History .....</b>	<b>2</b>
<b>1. Overview .....</b>	<b>1</b>
<b>2. Key Features .....</b>	<b>2</b>
<b>3. Package and Pin Distribution .....</b>	<b>4</b>
3.1 Package .....	4
3.2 Pin Distribution .....	6
<b>4. Hardware Features .....</b>	<b>7</b>
4.1 Welding process recommendations .....	7
4.2 Tide sensitive parameters .....	8
<b>5. Electrical performance .....</b>	<b>12</b>
5.1 Extreme working conditions .....	12
5.2 Recommended working conditions .....	12
5.3 DC gas parameters .....	12
<b>6. Ordering Information .....</b>	<b>14</b>
Chip identification and definition .....	14

# 1. Overview

The GK7205V210 chip is a new generation of low-power multimedia SOC chip that supports H.265 encoding from GOK.

The chip integrates a dedicated ISP with efficient video encoding processing performance and supports H.265 encoding to meet customers' various differentiated business needs. The integrated RTC, POR, Audio codec and rich peripheral interfaces help customers to reduce BOM cost, and the low-power CPU and low-power architecture help customers to reduce power consumption.



**Figure 0-1: GK7205V210 Function Block Diagram**

## 2. Key Features

### CPU

- ARM Cortex A7 @ 900MHz
- 32KB I-Cache, 32KB D-Cache, 128KB L2 Cache
- Integrated multimedia acceleration engine - NEON and hardware Java acceleration
- Integrated hardware floating point co-processor

### ADPCM

- Support Audio 3A (AEC/ANR/AGC)

### Video and graphics processing

- Support for multiple application analysis

### Storage interface and startup

- Embedded 512Mb DDR2
- Supports up to 1200Mbps
- Support SPI Nor Flash, maximum capacity 256MB
- Supports SPI Nand Flash with a maximum capacity of 1GB
- Supports eMMC 4.5, up to 2TB capacity
- Selectable boot from SPI Nor or SPI Nand or eMMC

### Video Encoding

- Support H.265/H.264 video encoding
  - ✓ Supports a maximum resolution of 2560x1440
- MJPEG/JPEG encoding support
- Support CBR/VBR/FIXQP/AVBR/QPMAP/CVBR

### Audio Codec

- Support software codec, support G.711/G.726,

- Support video, graphics PQ boost
- Support ISP

### Safe handling

- Supports AES/RSA and other algorithms
- HASH Support
- OTP support
- Support TRNG

### Audio and video interface

- Video Input
  - ✓ Supports MIPI, LVDS, HiSPI interfaces
  - ✓ Support various mainstream HD sensors
- Video Output
  - ✓ LCD output support
  - ✓ Supports BT656/BT1120 output
- Audio Interface
  - ✓ Supports mic/line in input
  - ✓ Support line out output
  - ✓ I2S support

### Peripherals & Others

- Supports one USB2.0 Host/Device interface
- Supports one SDIO2.0 with SD2.0 card
- Supports 10M/100M Ethernet with built-in EPHY
- Supports four PWMs
- Supports three UART interfaces

- Dual-channel SAR ADC support
- Multiple I2C interfaces; multiple GPIO interfaces
- SPI interface support
- Built-in high-precision RTC

## Physical Specifications

- Operating Voltage
  - ✓ Core Voltage: 0.9v
  - ✓ IO Voltage: 3.3v
  - ✓ SDRAM Voltage: 1.8v
- Package:
  - ✓ QFN 9mm \* 9mm, 88pins

## 3. Package and Pinouts

### 3.1 Package

GK7205V210 chip adopts QFN package, the package size is 9mm×9mm, the pin pitch is 0.35mm, the total number of pins is 88, please refer to the figure for the detailed package.

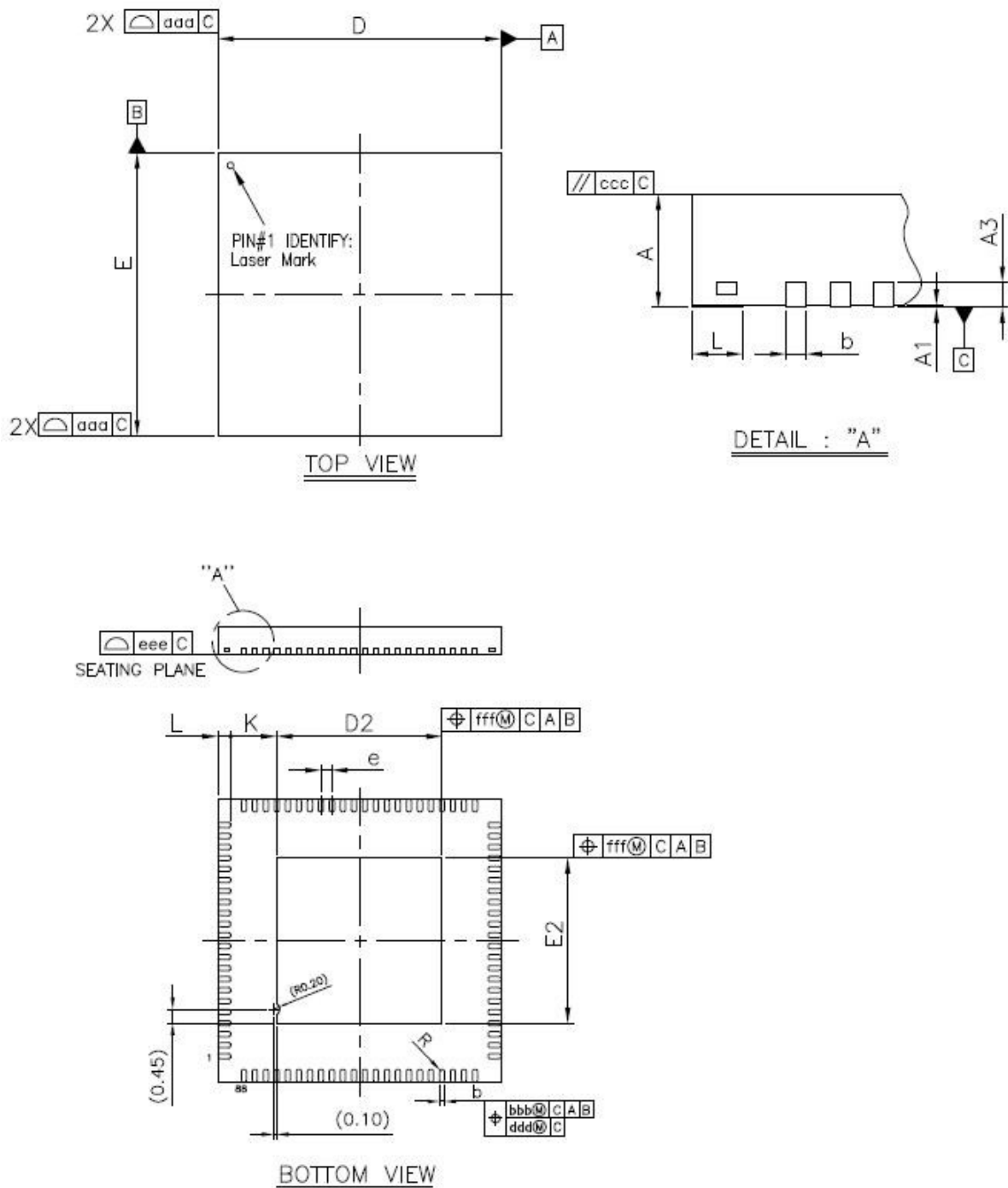


Figure 3- 1 GK7205V210 chip package diagram



Table 3-1 GK7205V210 chip package parameters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.11	0.16	0.21	0.004	0.006	0.008
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
D2	5.16	5.26	5.36	0.203	0.207	0.211
E2	5.16	5.26	5.36	0.203	0.207	0.211
e	0.35 BSC			0.014 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.055	---	0.105	0.002	---	0.004
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

## 3.2 Pin Distribution

PIN 1		88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67
		LSADC_CHO	LSADC_CHI	JTAG_TDO	JTAG_TDI	DVDD33	JTAG_TMS	JTAG_TCK	JTAG_TRSTN	VDD	VSS	VDDIO_DDR	VDD	AVDD33_DDR_PLI	VDDIO_DDR	UART0_RXD	UART0_TXD	GPIO0_0	PWM1	PWM0	SYS_RSTN_OUT	SFC_MOSI_IO0	SFC_CLK
1	AVDD_BAT	<div>GK7205V210</div>																				SFC_HOLD_IO3	66
2	RTC_XIN																					SFC_CSN	65
3	RTC_XOUT																					SFC_MISO_IO1	64
4	AVDD33_PLL																					SFC_WP_IO2	63
5	AVDD_PLL																					VDD	62
6	XIN																					SDIO0_CARD_DETECT	61
7	XOUT																					SDIO0_CDATA1	60
8	DVDD33																					DVDD3318_FLASH	59
9	LCD_DATA0																					SDIO0_CDATA0	58
10	LCD_DATA1																					SDIO0_CCLK_OUT	57
11	LCD_DATA2																					SDIO0_CCMD	56
12	LCD_DATA3																					SDIO0_CDATA3	55
13	VDD																					SDIO0_CDATA2	54
14	LCD_DATA4																					VDD	53
15	LCD_DATA5																					USB_DM	52
16	LCD_DATA6																					USB_DP	51
17	DVDD3318_VIVO																					AVDD33_AC_U2	50
18	LCD_DATA7																					AC_OUTL	49
19	LCD_CLK																					AC_MICBIAS	48
20	LCD_HS																					AC_INL	47
21	LCD_VS																					AC_VREF	46
22	LCD_DE																					AVSS_AC	45
		ETH_MDI_BN	ETH_MDI_BP	AVDD33_FE	ETH_MDI_AN	ETH_MDI_AP	ETH_LINK_ACT_LEI	ETH_LINK_STA_LEI	I2C2_SCL	I2C2_SDA	DVDD3318_SENSOR	I2C0_SDA	I2C0_SCL	SENSOR_CLK	SENSOR_RSTN	VDD	AVDD3318_MIPIRX	MIPI_RX_CROP	MIPI_RX_CHON	MIPI_RX_D0P	MIPI_RX_D0N	MIPI_RX_D2P	MIPI_RX_D2N
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Figure 3-2 GK7205V210 pinout diagram

## 4. Hardware Features

### 4.1 Welding process recommendations

#### 4.1.1 Lead-free reflow soldering process parameters requirements

The lead-free reflow soldering process profile is shown in Figure 4-1.

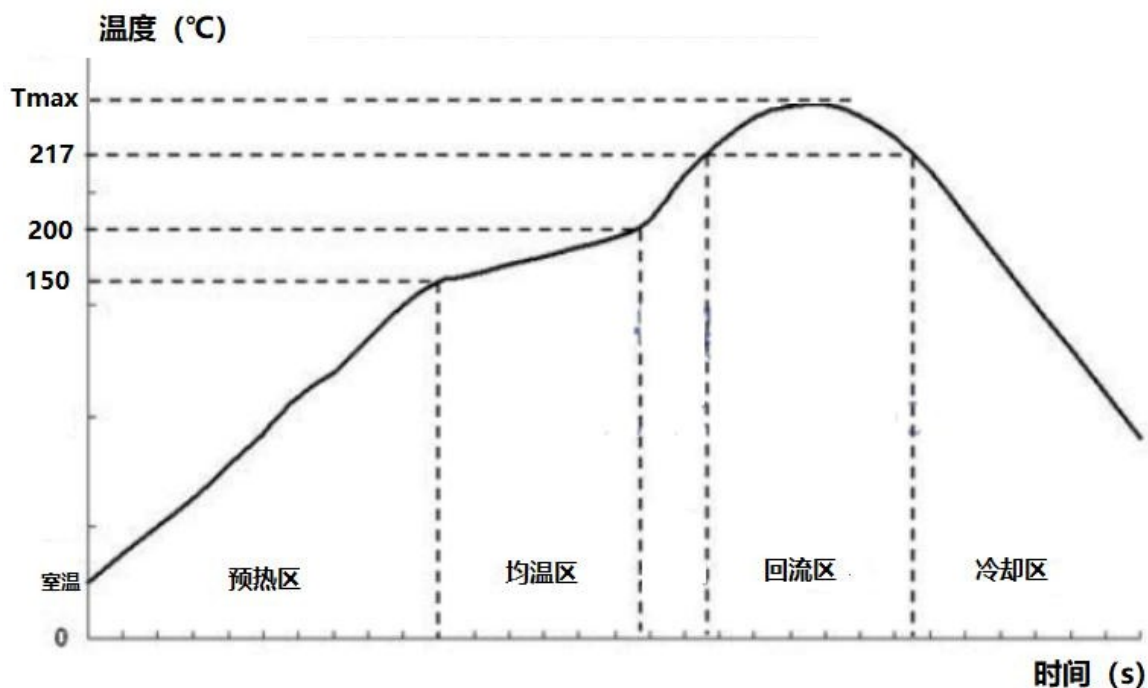


Figure 4-1. Lead-free reflow soldering process curve

Welding area	Time	Heating rate	Peak temperature	Cooling rate
Preheating zone (room temperature ~ 150°C)	60 to 150s	$\leq 2.0^{\circ}\text{C/s}$	-	-
Homogeneous temperature zone (150~200°C)	60 to 120s	$< 1.0^{\circ}\text{C/s}$	-	-
Reflux zone ( $> 217^{\circ}\text{C}$ )	60 to 90s	-	$T_{\text{max}} = 230\text{--}260^{\circ}\text{C}$	-

Cooling zone (Tmax ~ 180°C)	-	-	-	1.0°C/s≤Slope≤4.0°C/s
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Table 4-1 Lead-free reflow soldering process parameters

Lead-free reflow soldering process parameters are described:

Preheating zone: temperature from room temperature to 150 °C, the temperature rise rate is controlled at about 2 °C / s, the temperature zone time is 60 ~ 150s.

Even temperature zone: temperature from 150 °C ~ 200 °C, stable and slow heating, the temperature rise rate is less than 1 °C / s, and the region time control in 60 ~ 120 s (Note: the region must be slowly heated, otherwise it is easy to lead to poor welding).

Reflow zone: temperature from 217°C ~ Tmax ~ 217°C, the whole zone time control in 60~90s. 60~90s as the target of reflow time, for some heat capacity can not meet the time requirements of the veneer can be relaxed to 120s reflow time.

Cooling zone: temperature from Tmax to 180°C, the maximum temperature drop rate should not exceed 4°C/s. The total time for temperature rise from room temperature to Tmax should not exceed 6 minutes.

The reflow curve is only the recommended value, the client needs to make corresponding adjustments according to the actual production situation

## 4.2 Tide sensitive parameters

This section sets out the principles for the use of ICs (tide sensitive products) and covers the following explanation of terms:

- Floor life: the maximum time the product is allowed to remain in the workshop (ambient <30°C/60% RH, before unpacking the moisture-proof package to reflow)
- Desiccant (desiccant): a material used to adsorb moisture and keep it dry
- Humidity Indicator Card (HIC): Humidity Indicator Card
- Moisture sensitivity level (MSL): Moisture sensitivity level
- Moisture Barrier Bag (MBB): Moisture Barrier Bag
- Solder Reflow: Reflow soldering
- Shelf Life: normal storage time after moisture-proof packaging

【Tide Sensitive Grade

The moisture sensitivity level of this product is 3.

### 4.2.1 Product moisture-proof packaging

#### 4.2.1.1 Packaging Information

Dry vacuum packaging materials contain:

- Humidity Indicator Card (HIC)
- Moisture Barrier Bag (MBB)
- Desiccant

Figure 4-2 Schematic diagram of dry vacuum packaging materials



#### 4.2.1.2 Tide sensitive products incoming inspection

Prior to production use (SMT), after opening the vacuum bag:

- If the maximum indication point of the HIC has changed (not blue or earthen), the product must be rebake with reference to Table 4-3.
- If the 10% RH dot in the HIC is blue or earthy, the product is dry and can be vacuum sealed by simply replacing the moisture barrier.

### 4.2.2 Storage and Use

[Storage Environment]

It is recommended to store the product in vacuum packaging at <30°C/60% RH.

【shelf life】 (normal storage time after moisture-proof packaging)

Storage environment <30°C/60% RH, vacuum packaging storage, shelf life (storage period) of not less than 12 months.

【floor life

At ambient conditions <30°C/60%, floor life is referenced below.

Table 4-2 Floor life reference table

MSL	Floor life(out of bag) at factory ambient ≤30°C/60% RH or as stated
1	Unlimited at ≤30°C/85% RH

2	1 year
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MSL	Floor life(out of bag) at factory ambient $\leq 30^{\circ}\text{C}/60\% \text{ RH}$ or as stated
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use, must be reflowed within the time limit specified on the label

The use of [Chao Min products].

- If the product is exposed to  $\leq 30^{\circ}\text{C}/60\% \text{ RH}$  for more than 2 hours continuously or cumulatively, it is recommended to rebake and then vacuum dry the package.
- If the product is exposed under  $\leq 30^{\circ}\text{C}/60\% \text{ RH}$  for not more than 2 hours in total, it can be used without rebake, but it should be replaced with new desiccant and vacuum dried and packed.

For storage and usage principles not mentioned in this document, please refer directly to **JEDEC J-STD-033A**.

## 4.2.3 Re-baking

[Scope of Use]

ICs that need to be re-baked (moisture sensitive products)

[Re-baking reference table]

Table 4-3 Re-baking reference table

Body thickness	level	bake@ $125^{\circ}\text{C}$	bake@ $90^{\circ}\text{C} \leq 5\% \text{ RH}$	bake@ $40^{\circ}\text{C} \leq 5\% \text{ RH}$
$\leq 1.4\text{mm}$	2a	3 hours	11 hours	5 days
	3	7 hours	23 hours	9 days
	4	7 hours	23 hours	9 days
	5	7 hours	24 hours	10 days
	5a	10 hours	24 hours	10 days
$\leq 2.0\text{mm}$	2a	16 hours	2 days	22 days
	3	17 hours	2 days	23 days
	4	20 hours	3 days	28 days
	5	25 hours	4 days	35 days
	5a	40 hours	6 days	56 days
$\leq 4.5\text{mm}$	2a	48 hours	7 days	67 days

Body thickness	level	bake@125°C	bake@90°C≤5% RH	bake@40°C≤5% RH
	3	48 hours	8 days	67 days
	4	48 hours	10 days	67 days
	5	48 hours	10 days	67 days
	5a	48 hours	10 days	67 ays
Remarks	<p>This table shows the minimum baking time necessary after moisture. Re-baking preference is given to low temperature baking.</p> <p>Please refer to JEDEC for details</p>			

## 5. Electrical performance

### 5.1 Extreme working conditions

Permanent damage may occur if the chip is operated at maximum rated conditions beyond the limit operating conditions. Functional operation should be limited to the conditions given in the "Recommended Operating Conditions" section. Prolonged operation under extreme operating conditions may affect the reliability of the device. Chip junction temperatures exceeding destructive junction temperatures may result in physical damage to the chip.

Table 5- 1 Limiting operating conditions (VSS=0V)

Parameters	Symbols	Scope	Unit
Supply voltage	0V9	-0.2 to +1.17	V
	1V8	-0.2 to +2.16	
	3V3	-0.2 to +3.96	
Destructive junction temperature	T <sub>J</sub>	125	°C

### 5.2 Recommended working conditions

Table 5- 2 Recommended working conditions

Parameters	Symbols	Requirements			Unit
		Minimum value	Typical values	Maximum value	
Supply Voltage	0V9	TBD	0.9	TBD	V
	1V8	TBD	1.8	1.89	
	3V3	3.135	3.3	3.465	
Chip ambient temperature	T <sub>A</sub>	0	–	70	°C
Chip junction temperature	T <sub>J</sub>	0	–	105	°C

## 5.3 DC gas parameters

		Conditions	Minimum value	Typical values	Maximum value	Unit
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> voltage = 3.3V	2.4	–	–	V
Low level output voltage	V <sub>OL</sub>		–	–	0.4	
High level input voltage	V <sub>IH</sub>		2	–	–	

Low level input voltage	V <sub>IL</sub>	I <sub>O</sub> voltage = 1.8V	-	-	0.8	
High level output voltage	V <sub>OH</sub>		1.35	-	-	
Low level output voltage	V <sub>OL</sub>		-	-	0.4	
High level input voltage	V <sub>IH</sub>		1.27	-	-	
Low level input voltage	V <sub>IL</sub>		-	-	0.58	

Table 5- 3 DC Electrical Parameters

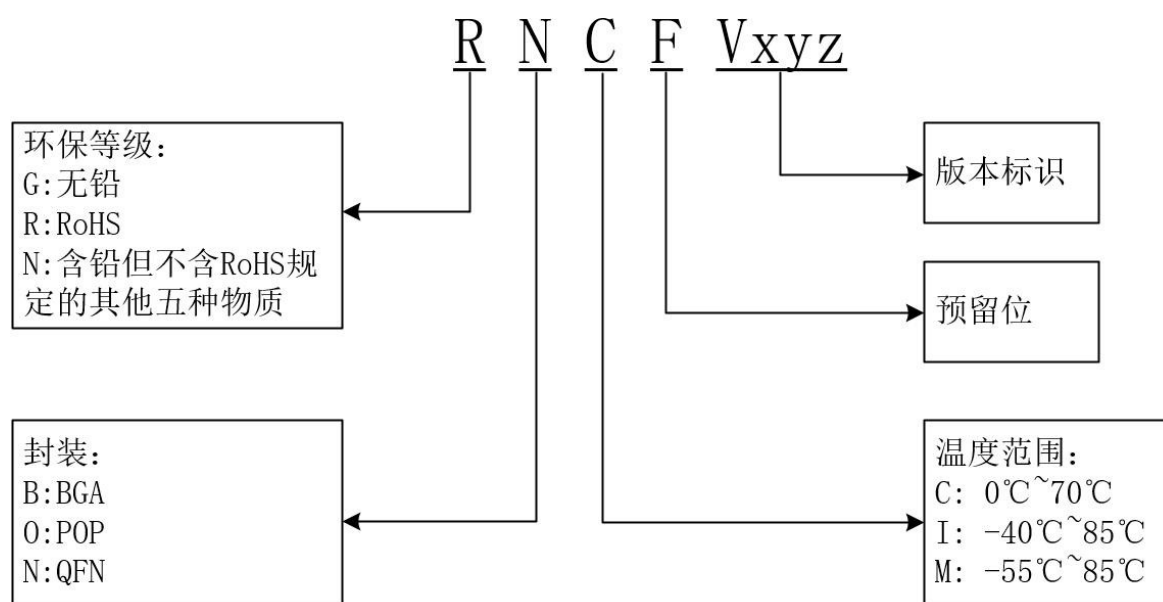
## 6. Ordering Information

### Chip identification and definition

Chip identification:



Extended bit definition:



## 7.RoHS Description

All GK7205V210 products provided to our customers are RoHS products, i.e., they are Lead-free.